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(54) Charging of a bootstrap capacitance through an LDMOS transistor

(57) A charging circuit for a bootstrap capacitance employing an integrated LDMOS transistor and including a circuital device for preventing the turning on of parasitic transistors of the integrated LDMOS structure during transients that comprises a plurality of directly biased junctions (D1, D2, ..., Dn) connected in series between a source and a body of the LDMOS transistor structure and at least a current generator, tied to ground potential, coupled between said body and ground, has at least one switch (INT1) between said source and a first junction (D1) of said plurality of junctions and a limiting resistance (R) connected between the body and the current generator (GEN). The switch (INT1) is kept open during a charging phase of the bootstrap capacitance (Cboot) and is closed when the charge voltage (Vboot) of the bootstrap capacitance reaches a preset threshold. Moreover, the body voltage (VB) is prevented from exceeding the source voltage (VS) plus a Vbe, by controlling a discharge path (T2) with a control stage (T1, R1) in response to a drop of the voltage on the limiting resistance (R). This body voltage control circuit is enabled by a second switch (INT2) driven in phase with the first switch (INT1).

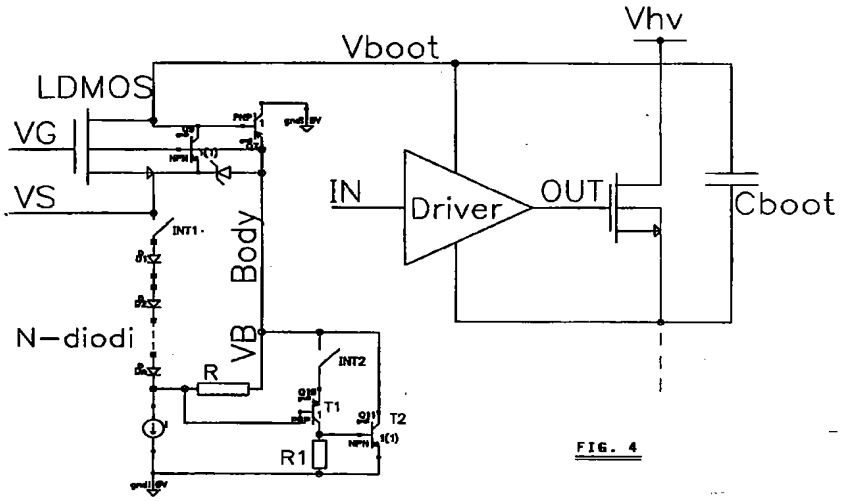

FIG. 4

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Description

The present invention is concerned with integrated circuit and more in particular with driving circuits of power stages. The invention refers to a bootstrap system whereby the capacitance is charged through an LDMOS integrated transistor.

In integrated circuits comprising output stages destined to drive discrete power devices or themselves integrated on the same chip containing the drive and control circuitry, it is common the employment of a bootstrap capacitance so as to ensure a correct supply of the driving stage of the power device. In this type of systems, it is essential to ensure the charge of the bootstrap capacitance in a very short period of time and it is also common the use of an LDMOS transistor in order to rapidly charge the bootstrap capacitance.

In the specific case of a driving circuit destined for a so-called High Side Driver (HSD), the LDMOS should be able to charge the bootstrap capacitance when the HSD is tied to the low voltage, that is when the output of the HSD is low. By contrast, when the HSD is tied to the high voltage, that is when the HSD output is high, the LDMOS should represent a high impedance. These operating conditions must be complied with even during the high-to-low voltage phase of commutation (or vice-versa) of the HSD itself regardless possible current injections originating from charging and discharging processes of capacitances associated to the integrated structure of the LDMOS that must withstand the high voltage supply of the power device.

In order to control the intrinsic parasitic effects of an integrated LDMOS structure, it is a well known practice the realization of an integrated structure represented by the circuit shown in Fig. 1. Typically, the driving voltage VG for the gate of the integrated LDMOS is obtained from the VS source voltage by means of a charging pump.

As a matter of example, the driving stage refers to an HSD that is driven in a turn-on or turn-off mode by a certain control signal IN. The HSD supply, when referred to high voltage (Vhv), is assured by the bootstrap capacitance Cboot. Moreover, during this phase, the bootstrap capacitance Cboot loses the electric charge necessary to the charging and consumption of the HSD.

During the phase where the output (OUT) of the HSD is low, the charging transistor LDMOS is turned on so as to restore the electric charge absorbed from the bootstrap capacitance Cboot in the preceding phase.

The n diodes (or junctions directly biased in series) have the specific function of impeding the turning-on of the parasitic PNP during the dynamic operation of the circuit. As a matter of fact, if the structure is dimensioned in such a way that Vboot>VS-(n+1)Vbe , the parasitic transistor PNP can not turn on.

When turning on the circuit, and before commuting the HSD output, it is necessary to charge the initially uncharged bootstrap capacitance Cboot.

Referring back to the circuital scheme of Fig. 1, it can be noticed that when VS>nVbe, the body node of the LDMOS transistor is at a voltage that satisfies the condition VB=VS-nVbe . If the voltage VS of the source node continues to rise faster than the voltage Vboot of the charging bootstrap capacitance, the parasitic PNP of the LDMOS integrated structure turns on, driving all or part of the current toward the integrated circuit substrate rather than in the Cboot capacitance. This implies the risk of not achieving the charging of the bootstrap capacitance or in any case to attain this in an excessive long period of time, moreover with a considerable waste of energy via the substrate.

Additional and more serious inconveniences may occur during the HSD commutation with this known type of circuit. This is due to the presence of a parasitic NPN associated with the integrated structure of the LDMOS.

If we consider the presence of the junction capacitance Cbd between the body and the drain as shown in Fig. 2, during the voltage rising front of the drain node of the LDMOS transistor occurs a current injection in the body through the Cbd capacitance of the body-drain junction.

If due to such a current injection the body potential VB rises above the value: VS+Vbe, by considering the design condition whereby:

$$Vboot > VS - (n + 1)\,Vbe \qquad (1)$$

the source-body junction is directly biased thus turning on the parasitic NPN transistor with the consequent destruction of the integrated component due to an extremely high power dissipation. This failure mechanism is very likely to occur since the body represents a high impedance node.

This demonstrates the utility of a charging circuit of a bootstrap capacitance using an integrated transistor LDMOS that would assure a low consumption and high immunity toward the occurrence of conditions that may the cause the destruction of the integrated device.

This object is fully reached by the present invention which relates to a method and to an implementing circuit capable of assuring the interdiction of parasitic transistors and a minimization of current leakage under all operating conditions of the charging circuit of a bootstrap capacitance using an LDMOS integrated transistor. According to an embodiment of the invention, a switch interrupts the connection between the source node and the first junction of the drain of directly biased junctions that commonly exists between the source node and a current generator linked to the ground potential, during the charging phase of the bootstrap capacitance. The switch is turned off when the voltage of the charging bootstrap capacitance reaches a pre-established threshold. Furthermore, the current that may accidentally be injected by the triggering of a parasitic transistor is limited in any case by employing a limiting resistance between the body node of the LDMOS

structure and the current generator itself, which is in turn linked to the circuit ground potential.

According to a further aspect of this invention, even a slight residual probability of the occurrence of conditions that would bring into a conductive state the parasitic NPN transistors; because, for example, of an injection of current during a commutation phase, via the capacitance between drain and body, can be effectively eliminated by employing an appropriate circuit able to prevent the body voltage to rise above the source voltage plus a Vbe. This is achieved by establishing a discharge path of the body node that is enabled by a driving stage responsive to a voltage drop sensed across the above mentioned limiting resistance connected in series with the body. This switched discharge circuit is enabled by a second switch that can be controlled in phase with the first switch by a control circuit in function of the actual voltage present on the bootstrap capacitance.

The various aspects and advantages of this invention will be more evident through the following description of some important though nonlimitative embodiments, and by referring to the annexed drawings, wherein:

Figures 1 and **2** represent partial diagrams illustrating the problems associated with a charging circuit of a bootstrap capacitance, as previously mentioned;
Figure 3 is a basic diagram of a charging circuit according to a first embodiment of this invention;
Figure 4 shows a basic diagram of a charging circuit according to an alternative embodiment realization of this invention;
Figure 5 is a circuit diagram of a sample embodiment of the present invention;
Figure 6 represents a block diagram of a device incorporating a driving circuit according to Fig. 5.

Referring to Fig. 3, we assume to be charging for the first time the bootstrap capacitance Cboot. In order that during the charging transient the parasitic PNP transistor does not turn on, it is necessary to maintain the body of the charging LDMOS transistor, that in turn constitutes the PNP's emitter, at a potential as low as possible (in practice to ground potential) until the source voltage VS exceeds the breakdown voltage of the parasitic zener. However, this procedure diminishes the ability of delivery current of the charging transistor LDMOS due to the body effect (increase of its own threshold). Therefore, it is of paramount importance that, once the charging process ends, the LDMOS transistor body be brought to a higher voltage. This is obtainable by means of the switch INT1.

The INT1 switch is kept open during the charging of the bootstrap capacitance (Cboot).

When the voltage Vboot reaches a level that fulfills the expression;

$$Vboot > VS - (n + 1)\,Vbe \qquad (1)$$

the INT1 switch is closed and the voltage of the body node can rise up to a point of complying with the following condition:

$$VB = VS - nVbe \qquad (2)$$

without determining the triggering of any parasitic transistor.

The resistance R, connected in series with the body functions as current limiter in the case where the above condition (1) can not be fulfilled due to accidental causes (noise) or otherwise whereby the switch INT1 be turned off too early. In any case the consumption of current via the substrate that would be caused by the triggering-on of the parasitic PNP transistor will be limited in function of the value of the limiting resistance R.

According to an alternative and preferred embodiment of this invention, the drawbacks deriving from current injection during commutation phases through the parasitic capacitance existing between the drain and body of the LDMOS structure, which under certain operating conditions may determine the triggering-on of the parasitic NPN transistor, are effectively overcome by adding a circuit that prevents the body voltage VB from exceeding the source voltage VS plus a Vbe. This is obtained by establishing a discharge path of the body node through a transistor T2 controlled by a driving stage, made up, for example, by T1 and R1, in response to the voltage drop occurring at the terminals of the current limiting resistance R. An additional second switch INT2, driven in phase with the INT1 switch, enables the driving stage T1-R1 when the bootstrap capacitance Cboot has reached a situation of full charge.

Assuming the INT2 switch closed, if the body potential VB (initially having a value equal to Vs-nVbe) raises by just one Vbe, in other words if it reaches a value given by VS-(n-1) Vbe, during a "low" to "high" transient of the output, the PNP transistor T1 turns on turning on the NPN transistor T2 that provides a discharge path of the body potential. In this way, the source/body junction cannot become directly biased and therefore the parasitic PNP transistor does not turn on. Of course, the discharge circuit should be designed in such a way to possess an adequate commutation speed, bearing also in mind the electrical characteristics of the integrated structure of the charging LDMOS.

The function of the switch INT2 that activates the driving stage T1-R1 is that of limiting current consumption.

Indeed, during a first charging phase of the bootstrap capacitance Cboot, the body of the LDMOS transistor is kept at ground potential by using a current generator GEN. If the source voltage VS exceeds the breakdown voltage (VZ) of the body-source junction, then the body would attain the voltage given by VS-VZ due to the high impedance of the current generator GEN that is in turn connected in series to the limiting

resistance R. When the circuit condition VS-VZ>Vbe is met, the discharge circuit, made up of the transistors T1 and T2 would absorb much current which in turn would leak toward the substrate. By inserting a switch INT2, that can be driven in phase with INT1, that is by keeping the switch INT2 open while INT1 is open, the transistors T1 and T2 remain turned off during the charging process of the bootstrap capacitance, avoiding so any loss of current.

The control of the switch INT1 or that of the switches INT1 and INT2 together, is easily attainable by means of a simple driving circuit responding to the instantaneous value of the voltage (Vboot) present on the charging bootstrap capacitance.

A sample of the circuital realization of the present invention is schematically shown in Fig. 5, the figure includes also a timing and a control circuit of the INT1 and INT2 switches. The comparator COMP senses the voltage Vboot-Vout, however, before the systems starts to commute, Vout is necessarily linked at ground potential or at a value very close to zero, therefore when Vboot>Vref (with VS-(n+1)Vbe<Vref<Vs), on the resistance RIs a logic signal going from "0" to "1" is generated. If in the instance of VIs="1", VS is such that the system can start commuting (in other words when the "under voltage lockout' signal is equal to "1"), then the two PNP transistors that implement the switches INT1 and INT2 are commanded to turn on (in other words their control gate is biased to zero potential) assuring so a correct control (disabling) of the parasitic elements of the integrated LDMOS structure.

Fig. 6 shows a block diagram of a typical device for driving a push-pull power stage employing discrete power devices supplied at a voltage higher than the supply voltage of the control and driving circuitry. In Fig. 6 the thick black square individuate an integrated circuit contained in the device. In the device configuration shown in Fig. 6, during the entire stand-by phase, that is when LVG="1" and HVG="0", the bootstrap capacitance Cboot charges through the low-side power device, which is turn referred to ground potential, and through the integrated transistor LDMOS. During switching it is positively excluded that the HVG and the LVG be simultaneously "low" or "high". The bootstrap LDMOS is turned-on in phase with the LVG pin so as to assure the restoring of the charge in the bootstrap capacitance Cboot; charge that was lost by the bootstrap capacitance during a HVG="1" and LVG="0" phase.

Evidently, the driven load (LOAD) can be the winding of an electric motor, a solenoid of an actuator, a neon lamp or the like.

Claims

1. A charging circuit for a bootstrap capacitance (Cboot) employing an integrated LDMOS transistor and including a circuital device for preventing the turning on of a parasitic PNP transistor of the LDMOS structure during transients, comprises n directly biased junctions (D1, D2, ..., Dn) between a source node and a body node of the LDMOS transistor and at least a current generator (GEN), tied to the ground potential of the circuit, functionally connected between said body node and a ground node, characterized by comprising

   at least one switch (INT1) between said source node and a first junction (D1) of said n directly biased junctions;
   a limiting resistance (R) connected between said body node and said current generator (GEN);
   said switch (INT1) being kept open during a charging phase of said bootstrap capacitance (Cboot) and being closed when the charge voltage (Vboot) of the bootstrap capacitance (Cboot) reaches a pre-established threshold.

2. A charging circuit according to claim 1, wherein the above mentioned pre-established threshold is greater or equal to VS-(n+1)Vbe, where VS is the source voltage of the LDMOS.

3. A charging circuit according to claim 1, characterized in that it comprises a circuit capable of preventing the body voltage (VB) from exceeding the source voltage (VS) plus a Vbe, by establishing a discharge path (T2) of said body enabled by a control stage (T1, R1) in response to a voltage drop detected on said limiting resistance (R).

4. A charging circuit according to claim 3, characterized in that said control stage (T1, R1) comprises a second enabling switch (INT2) which is driven in phase with said first switch (INT1).

5. A charging circuit according to claim 1, characterized in that said first switch (INT1) is driven by a control circuit responding to the charge voltage (Vboot) of the bootstrap capacitance (Cboot).

6. A charging circuit according to claim 5, characterized in that said control circuit comprises a comparator (COMP), a level shifter circuit (LEVEL SHIFTER) driven by the output of said comparator (COMP) and capable of forcing a current through a resistance (RIs) connected between the output node of said level shifter circuit and a ground node;
   one logic NAND gate or equivalent having a first input coupled to said resistance (RIs), a second input controlled by an enabling logic signal and an output coupled to a control terminal of said first switch (INT1).

7. A charging circuit according to claims 4 and 6, whereby the output of said gate is coupled to the control terminals of said first (INT1) and second (INT2) switches.

8. An integrated device for driving a push-pull power stage made of a pair of discrete field effect power transistors supplied at a voltage higher than the supply voltage of the integrated driving circuit, comprising charging circuit of an externally connected bootstrap capacitance providing for the supply of a driving stage of the discrete power transistor tied to said high voltage, characterized in that said external bootstrap capacitance is charged by a circuit as specified in any of the preceding claims.

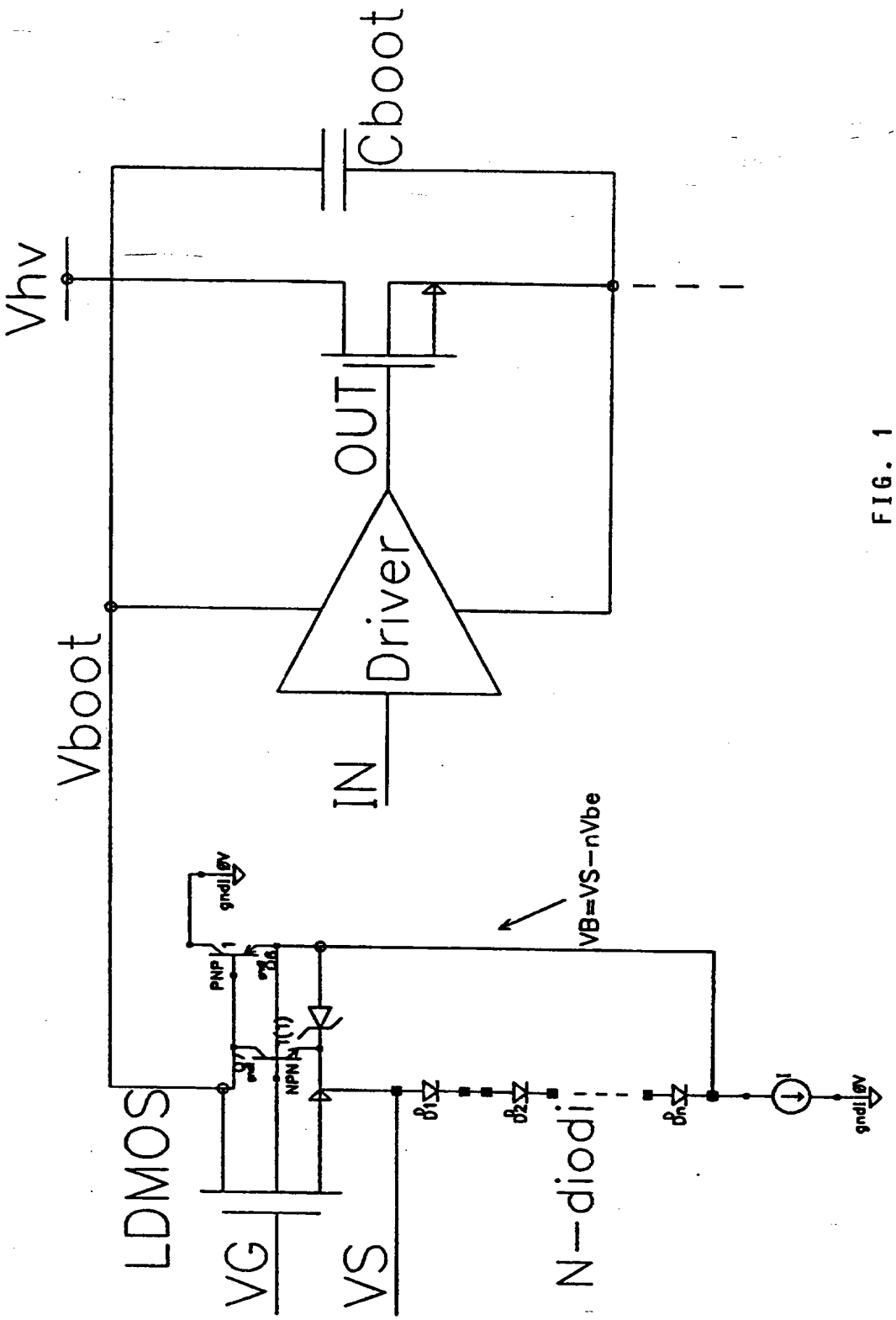

FIG. 1

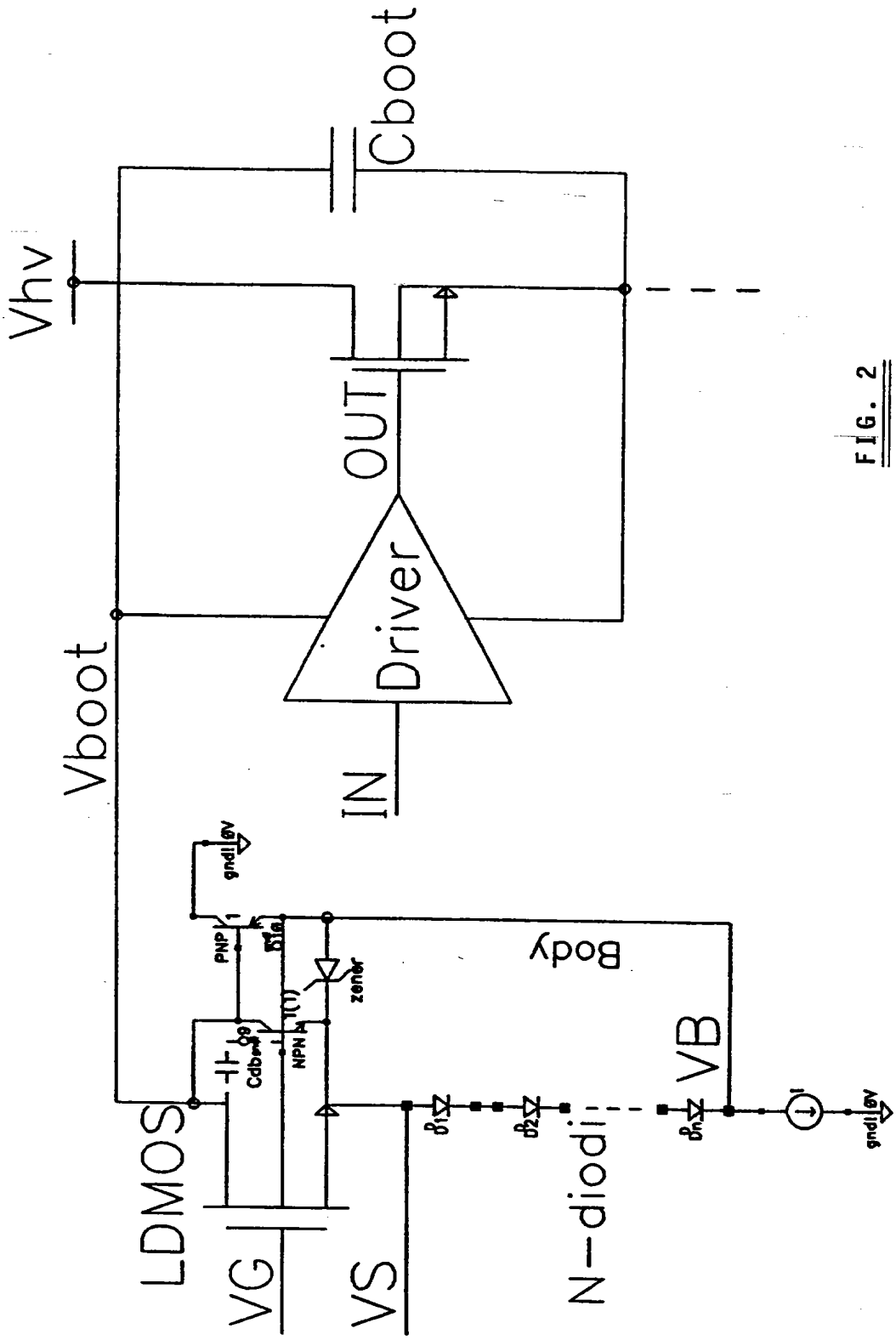

FIG. 2

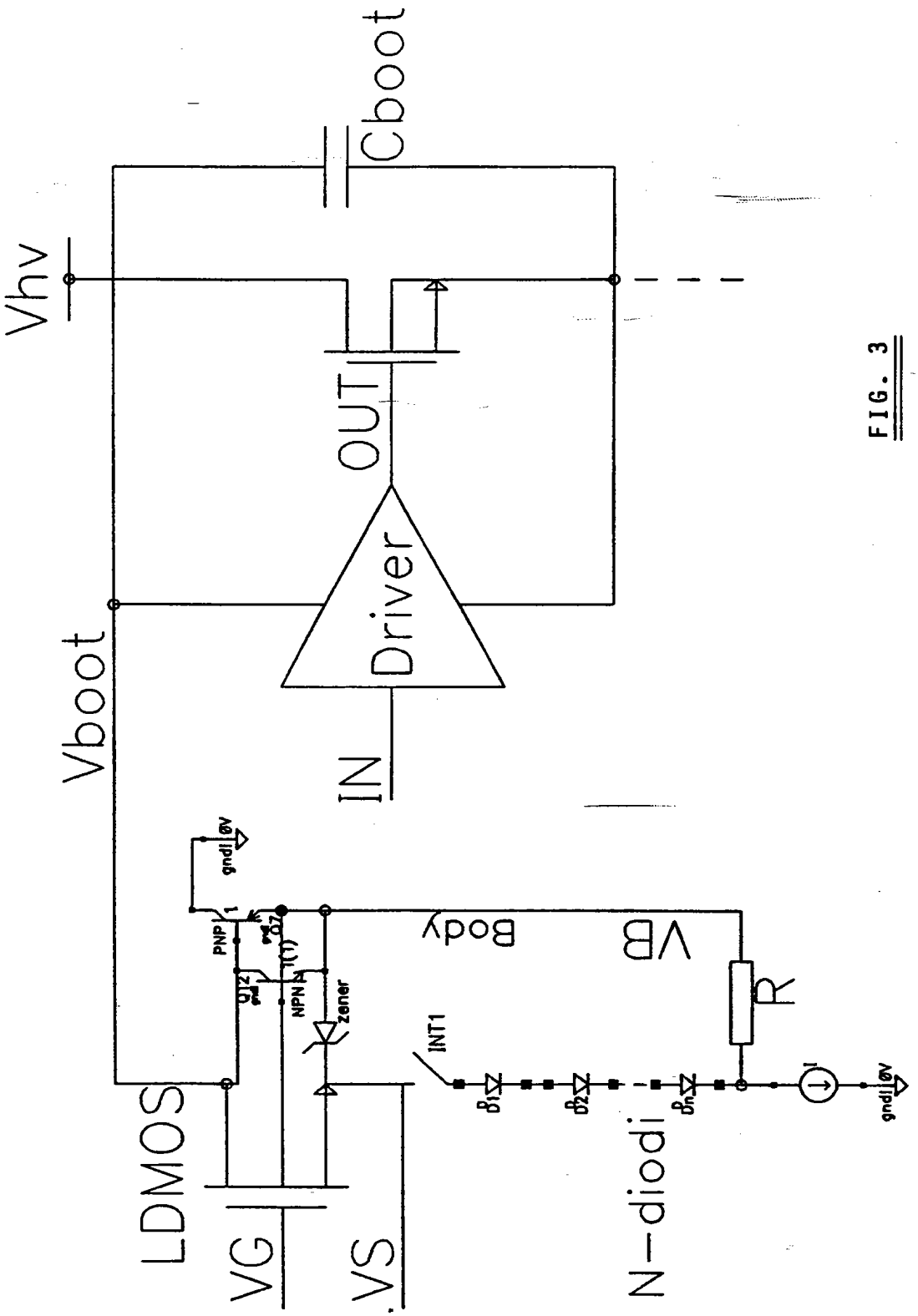

FIG. 3

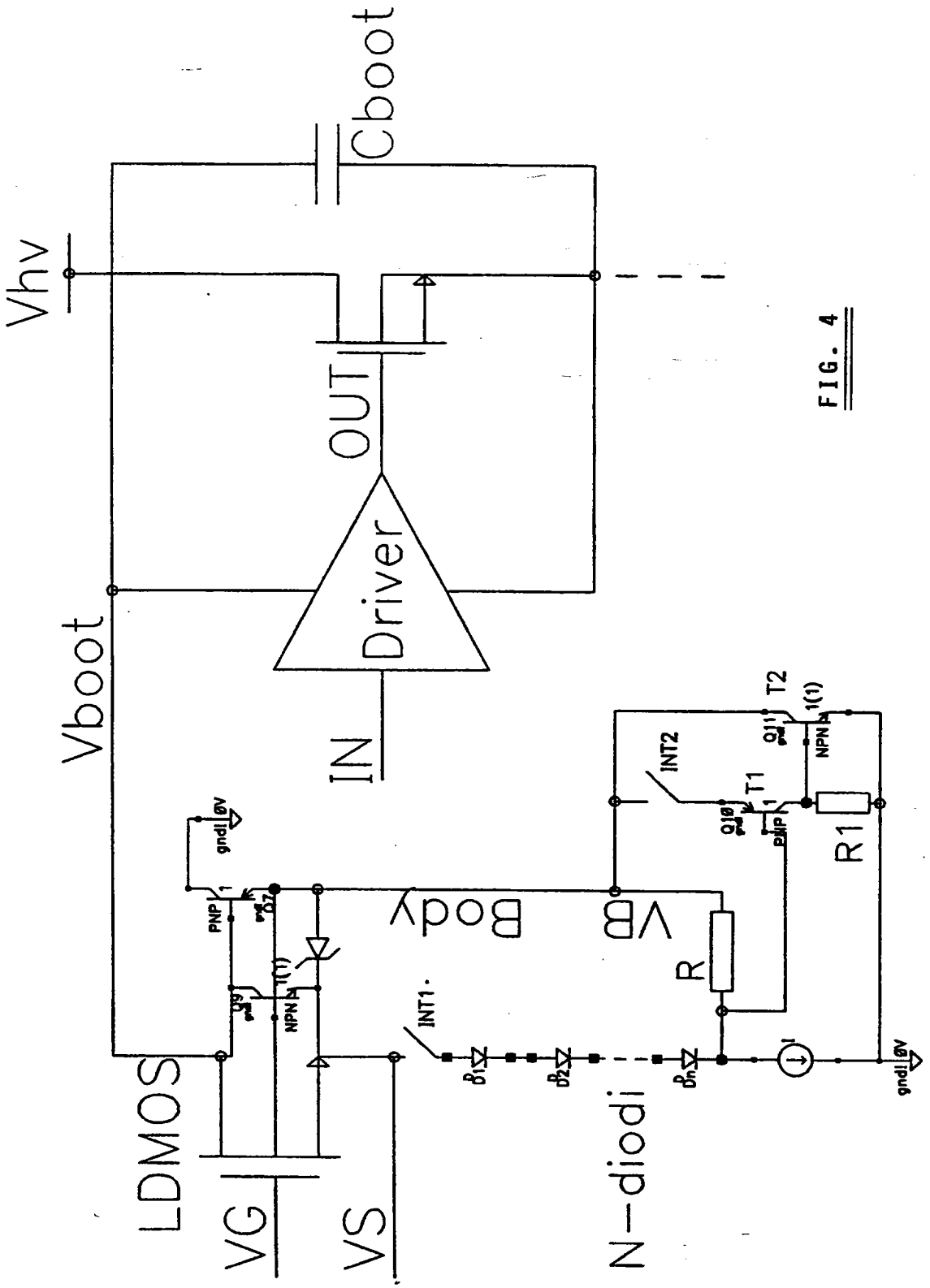

FIG. 4

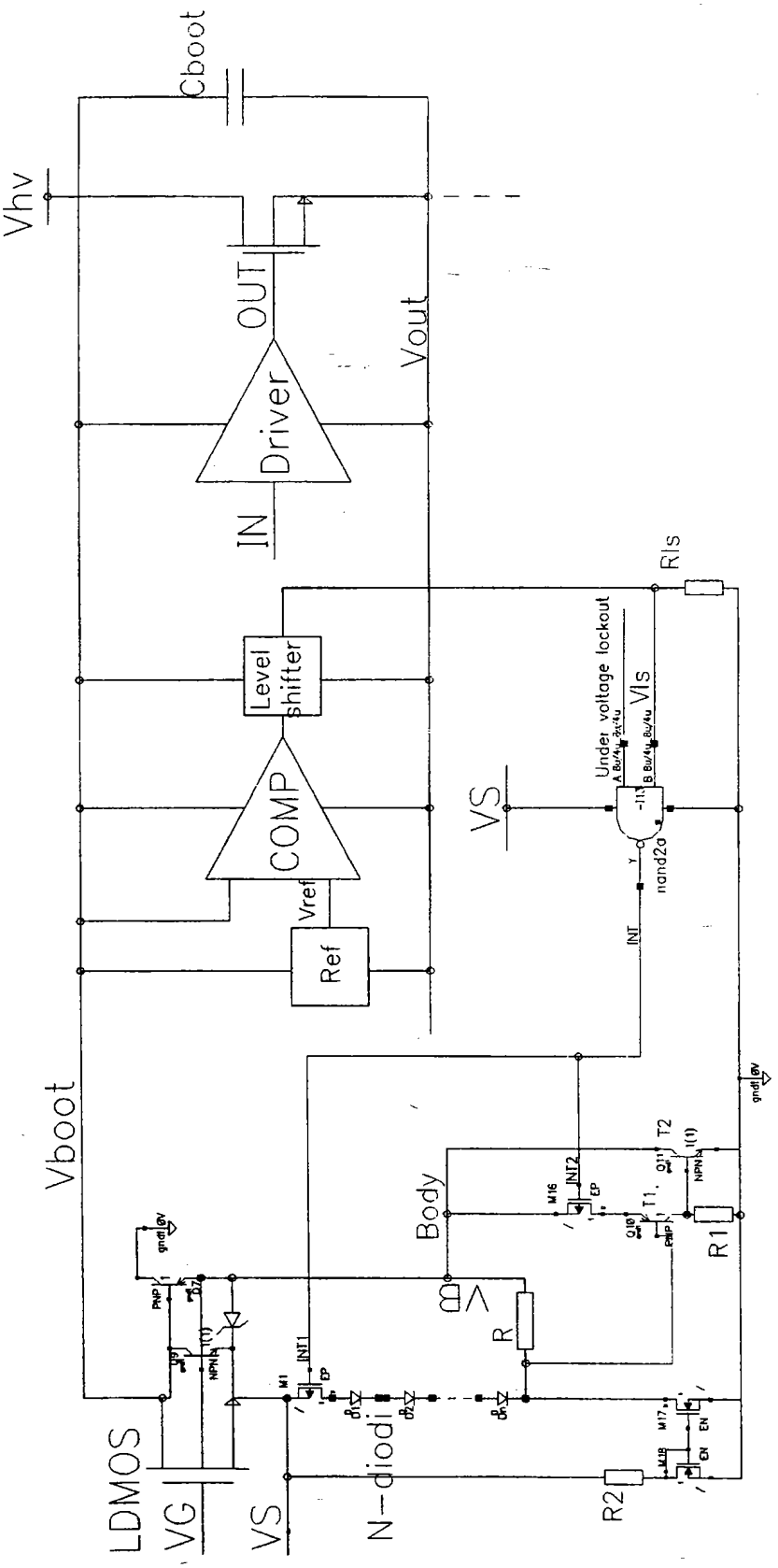

FIG. 5

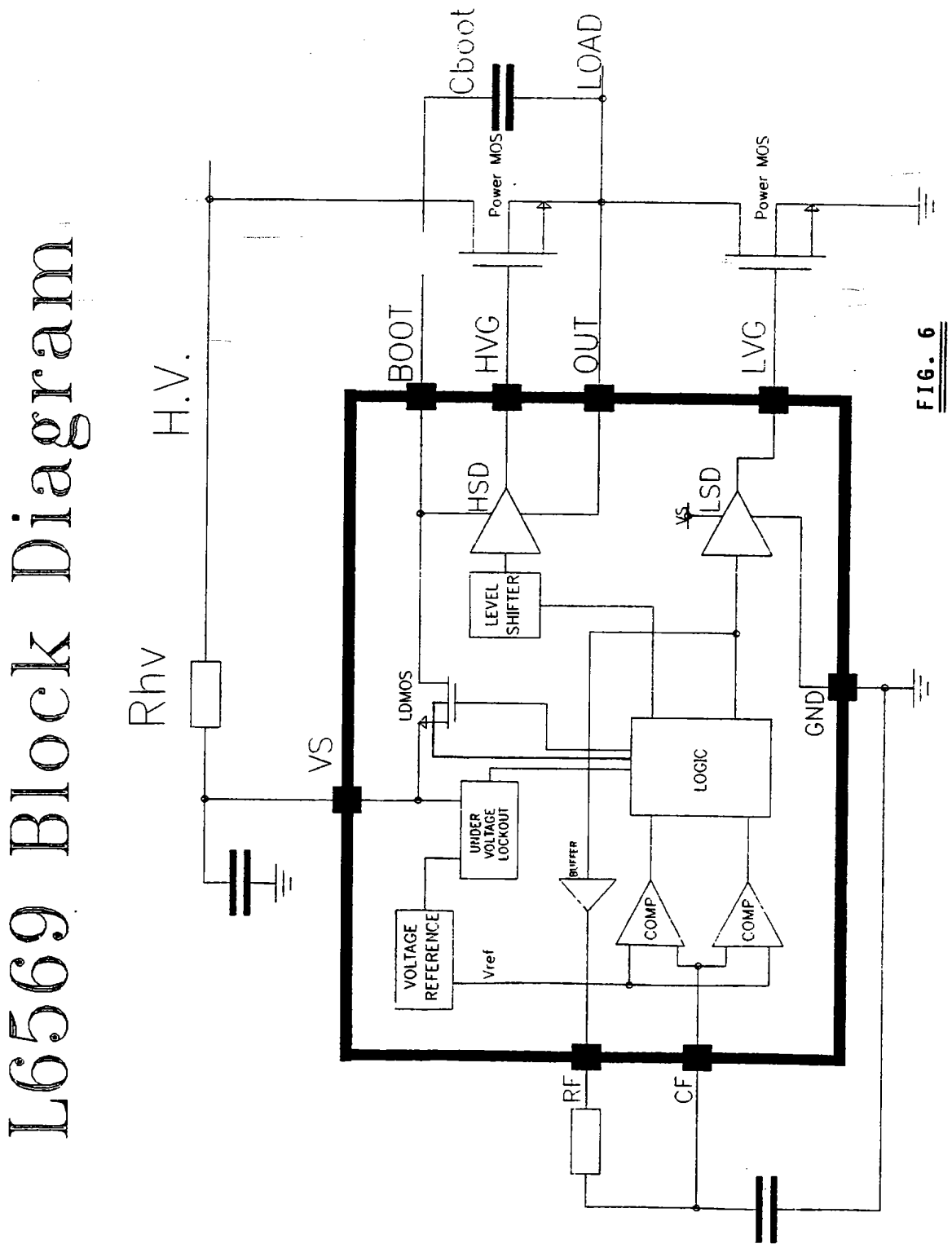

FIG. 6

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EUROPEAN SEARCH REPORT

Application Number
EP 95 83 0207

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	WO-A-94 27370 (PHILIPS ELECTRONICS N. V.) * abstract; figure 1 * ---	1,8	H03K17/687 H03K17/081
A	EP-A-0 367 006 (SGS-THOMSON MICROELECTRONICS S. P. A.) * abstract; figure 3 * -----	1,8	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	19 October 1995	Arendt, M

CATEGORY OF CITED DOCUMENTS

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